

Tikrit university

Collage of Engineering Shirqat

Department of Electrical Engineering

Second Class

Electronic I

Chapter 4

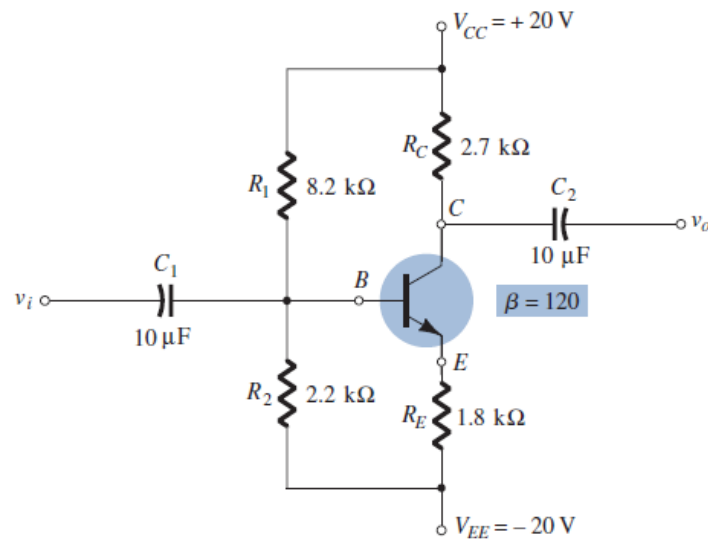
DC Biasing—BJTs

Prepared by

Lec 6

Asst Lecturer. Ahmed Saad Names

**EXAMPLE 20** Determine  $V_C$  and  $V_B$  for the network of Fig. 55.



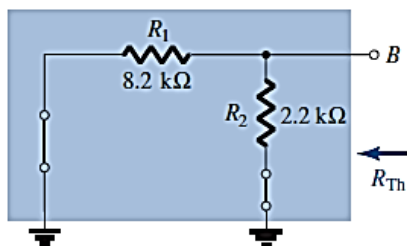
**FIG. 55**

Example 20.

**Solution:** The Thévenin resistance and voltage are determined for the network to the left of the base terminal as shown in Figs. 56 and 57.

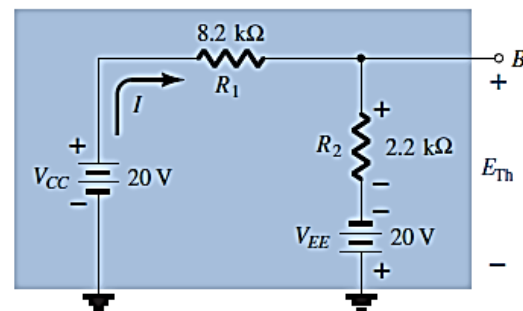
$R_{Th}$

$$R_{Th} = 8.2 \text{ k}\Omega \parallel 2.2 \text{ k}\Omega = 1.73 \text{ k}\Omega$$



**FIG. 56**

Determining  $R_{Th}$ .



**FIG. 57**

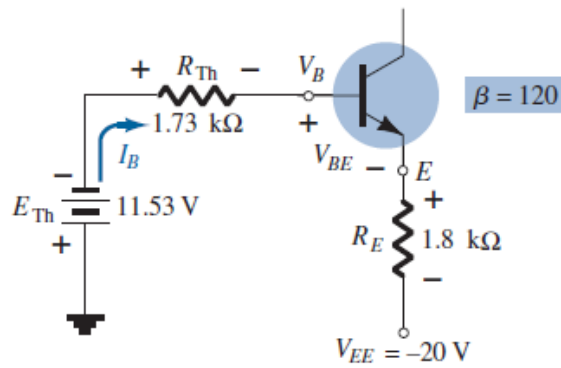
Determining  $E_{Th}$ .

$E_{Th}$ 

$$\begin{aligned}
 I &= \frac{V_{CC} + V_{EE}}{R_1 + R_2} = \frac{20 \text{ V} + 20 \text{ V}}{8.2 \text{ k}\Omega + 2.2 \text{ k}\Omega} = \frac{40 \text{ V}}{10.4 \text{ k}\Omega} \\
 &= 3.85 \text{ mA} \\
 E_{Th} &= IR_2 - V_{EE} \\
 &= (3.85 \text{ mA})(2.2 \text{ k}\Omega) - 20 \text{ V} \\
 &= -11.53 \text{ V}
 \end{aligned}$$

The network can then be redrawn as shown in Fig. 58, where the application of Kirchhoff's voltage law results in

$$-E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E + V_{EE} = 0$$

**FIG. 58**

*Substituting the Thévenin equivalent circuit.*

Substituting  $I_E = (\beta + 1)I_B$  gives

$$V_{EE} - E_{Th} - V_{BE} - (\beta + 1)I_B R_E - I_B R_{Th} = 0$$

and

$$\begin{aligned}
 I_B &= \frac{V_{EE} - E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} \\
 &= \frac{20 \text{ V} - 11.53 \text{ V} - 0.7 \text{ V}}{1.73 \text{ k}\Omega + (121)(1.8 \text{ k}\Omega)} \\
 &= \frac{7.77 \text{ V}}{219.53 \text{ k}\Omega} \\
 &= 35.39 \mu\text{A}
 \end{aligned}$$

$$\begin{aligned}
 I_C &= \beta I_B \\
 &= (120)(35.39 \mu\text{A}) \\
 &= 4.25 \text{ mA}
 \end{aligned}$$

$$\begin{aligned}
 V_C &= V_{CC} - I_C R_C \\
 &= 20 \text{ V} - (4.25 \text{ mA})(2.7 \text{ k}\Omega) \\
 &= 8.53 \text{ V}
 \end{aligned}$$

$$\begin{aligned}
 V_B &= -E_{Th} - I_B R_{Th} \\
 &= -(11.53 \text{ V}) - (35.39 \mu\text{A})(1.73 \text{ k}\Omega) \\
 &= -11.59 \text{ V}
 \end{aligned}$$

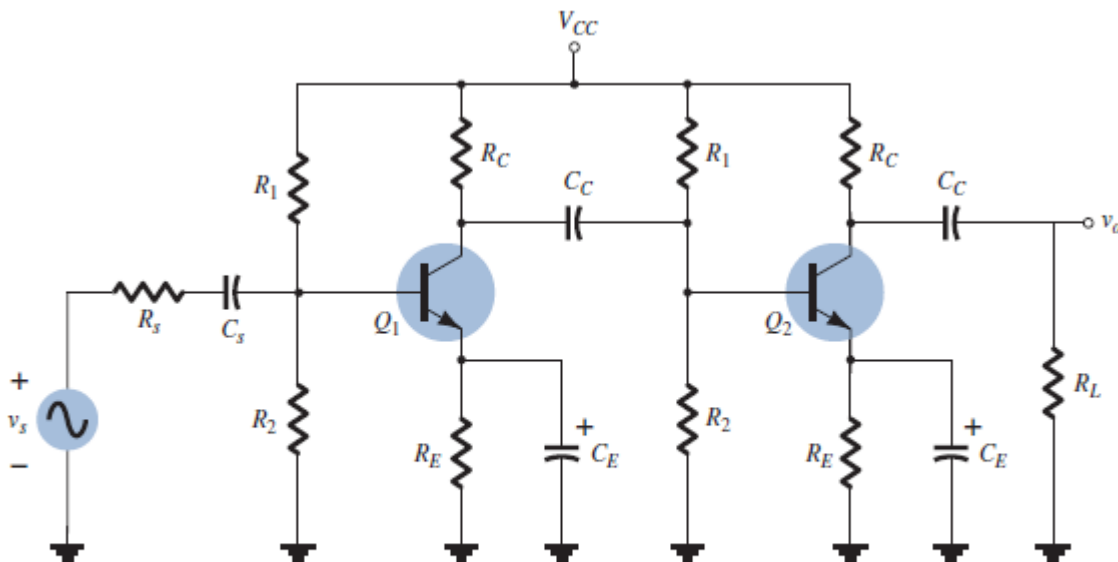
## 4.10 MULTIPLE BJT NETWORKS (Multistage)

The BJT networks introduced thus far have only been single-stage configurations. This section will cover some of the most popular networks using multiple transistors. It will demonstrate how the methods introduced thus far in this chapter can be applied to networks with any number of components.

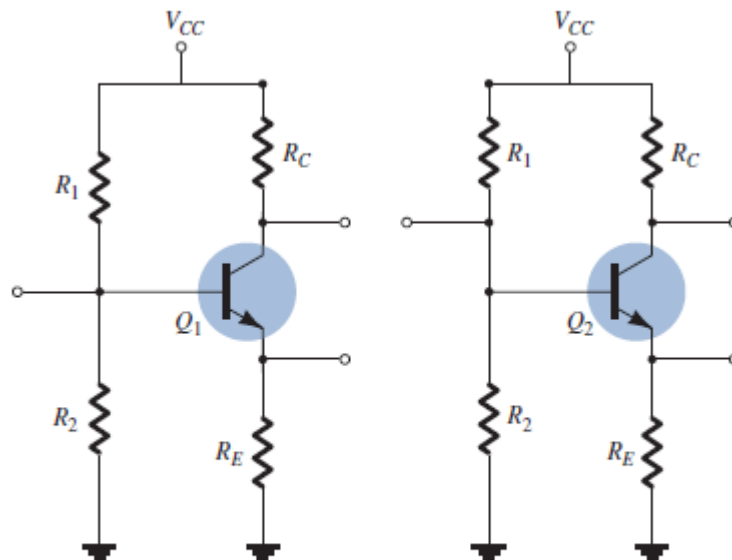
### 1. R–C coupling.

The R–C coupling of Fig. 64 is probably the most common. The collector output of one stage is fed directly into the base of the next stage using a coupling capacitor  $C_C$ . The capacitor is chosen to ensure that it will block dc between the stages and act like a short circuit to any ac signal. The network of Fig. 64 has two voltage-divider stages, but the same coupling can be used between any combination of networks such as the fixed-bias or emitter-follower configurations.

Substituting an open-circuit equivalent for  $C_C$  and the other capacitors of the network will result in the two bias arrangements shown in Fig. 65. The methods of analysis introduced in this chapter can then be applied to each stage separately since one stage will not affect the other. Of course, the 20 V dc supply must be applied to each isolated component.



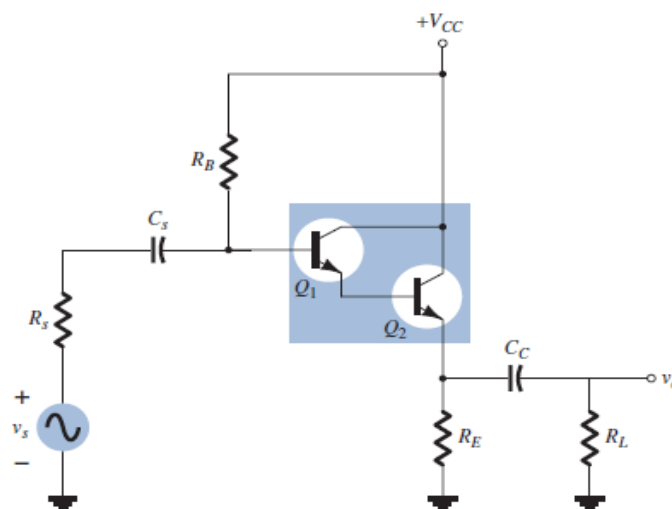
**FIG. 64**  
*R–C coupled BJT amplifiers.*



**FIG. 65**  
DC equivalent of Fig. 64.

## 2. Darlington

The Darlington configuration of Fig. 66 feeds the output of one stage directly into the input of the succeeding stage. Since the output of Fig. 66 is taken directly off the emitter terminal, you will find in the chapter “BJT AC Analysis” that the ac gain is very close to 1 but the input impedance is very high, making it attractive for use in amplifiers operating off sources that have a relatively high internal resistance. If a load resistor were added to the collector leg and the output taken off the collector terminal, the configuration would provide a very high gain.



**FIG. 66**  
Darlington amplifier.

For the dc analysis of Fig. 67 assuming a beta  $\beta_1$  for the first transistor and  $\beta_2$  for the second, the base current for the second transistor is

$$I_{B2} = I_{E1} = (\beta_1 + 1) I_{B1}$$

and the emitter current for the second transistor is

$$I_{E2} = (\beta_2 + 1) I_{B2} = (\beta_2 + 1) (\beta_1 + 1) I_{B1}$$

Assuming  $\beta \gg 1$  for each transistor, we find the net beta for the configuration is

$$\beta_D = \beta_1 \beta_2 \quad (50)$$

which compares directly with a single-stage amplifier having a gain of  $\beta_D$ . Applying an analysis similar to that of Section 4 will result in the following equation for the base current:

$$I_{B1} = \frac{V_{CC} - V_{BE1} - V_{BE2}}{R_B + (\beta_D + 1)R_E}$$

Defining

$$V_{BE_D} = V_{BE1} + V_{BE2} \quad (51)$$

we have

$$I_{B1} = \frac{V_{CC} - V_{BE_D}}{R_B + (\beta_D + 1)R_E} \quad (52)$$

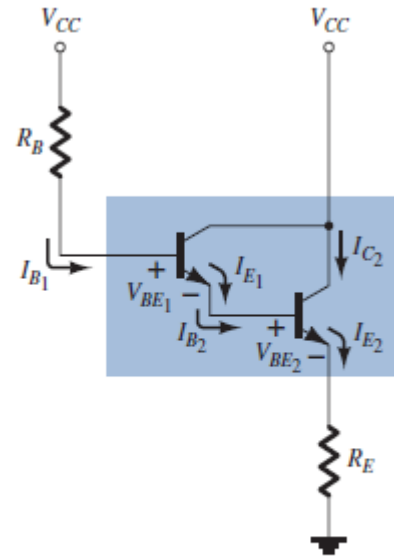
The currents

$$I_{C2} \cong I_{E2} = \beta_D I_{B1} \quad (53)$$

$$V_{E2} = I_{E2} R_E \quad (54)$$

$$V_{C2} = V_{CC} \quad (55)$$

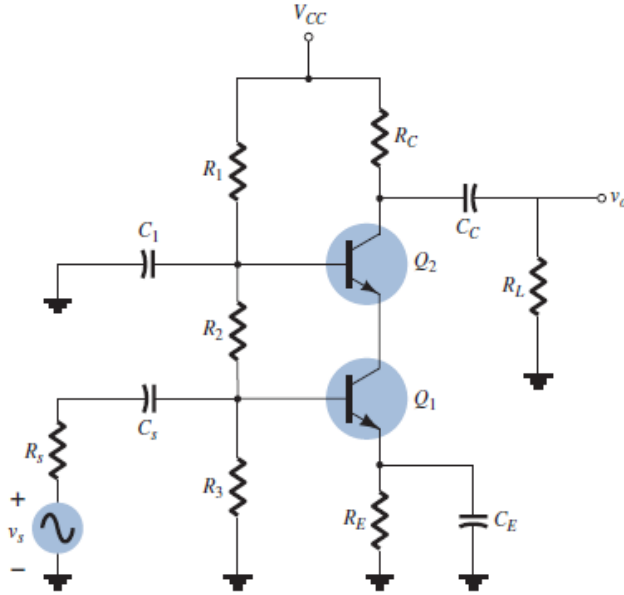
$$V_{CE2} = V_{CC} - V_{E2} \quad (56)$$



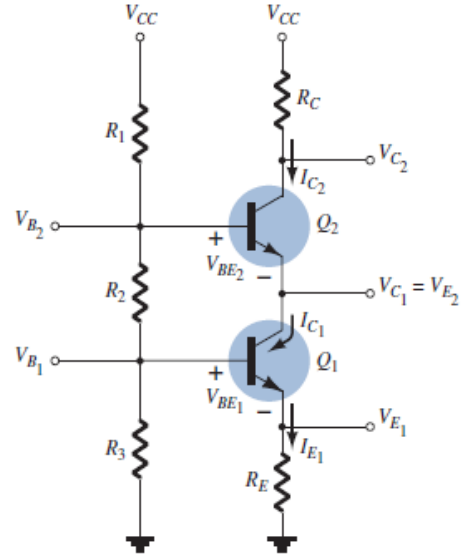
**FIG. 67**  
DC equivalent of Fig. 66.

### 3. Cascode

The Cascode configuration of Fig. 68 ties the collector of one transistor to the emitter of the other. In essence it is a voltage-divider network with a common-base configuration at the collector.



**FIG. 68**  
Cascode amplifier.



**FIG. 69**  
DC equivalent of Fig. 68.

The dc analysis is initiated by assuming the current through the bias resistors  $R_1$ ,  $R_2$ , and  $R_3$  of Fig. 69 is much larger than the base current of each transistor. That is,

$$IR_1 \approx IR_2 \approx IR_3 \gg I_{B1} \text{ or } I_{B2}$$

The result is that the voltage at the base of the transistor  $Q_1$  is simply determined by an application of the voltage-divider rule:

$$V_{B1} = \frac{R_3}{R_1 + R_2 + R_3} V_{CC} \quad (57)$$

The voltage at the base of the transistor  $Q_2$  is found in the same manner:

$$V_{B2} = \frac{(R_2 + R_3)}{R_1 + R_2 + R_3} V_{CC} \quad (58)$$

$$V_{E1} = V_{B1} - V_{BE1} \quad (59)$$

$$V_{E2} = V_{B2} - V_{BE2} \quad (60)$$

with the emitter and collector currents determined by:

$$I_{C_2} \cong I_{E_2} \cong I_{C_1} \cong I_{E_1} = \frac{V_{B_1} - V_{BE_1}}{R_E} \quad (61)$$

The collector voltage  $V_{C_1}$ :

$$V_{C_1} = V_{B_2} - V_{BE_2} \quad (62)$$

and the collector voltage  $V_{C_2}$ :

$$V_{C_2} = V_{CC} - I_{C_2}R_C \quad (63)$$

The current through the biasing resistors is

$$I_{R_1} \cong I_{R_2} \cong I_{R_3} = \frac{V_{CC}}{R_1 + R_2 + R_3} \quad (64)$$

and each base current is determined by

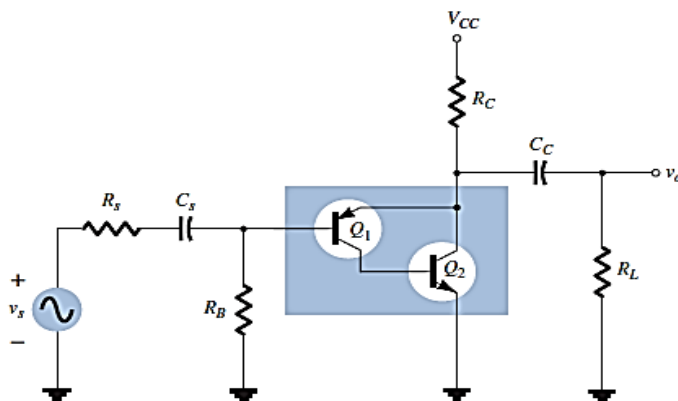
$$I_{B_1} = \frac{I_{C_1}}{\beta_1} \quad (65)$$

with

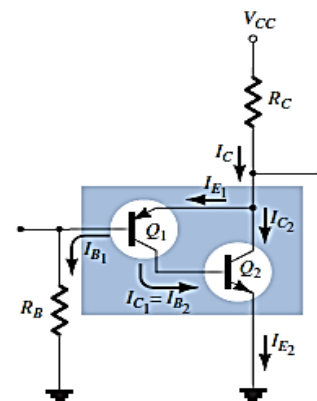
$$I_{B_2} = \frac{I_{C_2}}{\beta_2} \quad (66)$$

#### 4. Feedback Pair Amplifier

The next multistage configuration to be introduced is the Feedback Pair of Fig. 70, which employs both an npn and pnp transistor. The result is a configuration that provides high gain with increased stability. The dc version with all the currents labelled appears in Fig. 71.



**FIG. 70**  
Feedback Pair amplifier



**FIG. 71**  
DC equivalent of Fig. 70.



The base current

$$I_{B_2} = I_{C_1} = \beta_1 I_{B_1}$$

and

$$I_{C_2} = \beta_2 I_{B_2}$$

so that

$$I_{C_2} \cong I_{E_2} = \beta_1 \beta_2 I_{B_1} \quad (67)$$

The collector current

$$\begin{aligned} I_C &= I_{E_1} + I_{E_2} \\ &\cong \beta_1 I_{B_1} + \beta_1 \beta_2 I_{B_1} \\ &= \beta_1 (1 + \beta_2) I_{B_1} \end{aligned}$$

so that

$$I_C \cong \beta_1 \beta_2 I_{B_1} \quad (68)$$

Applying Kirchhoff's voltage law down from the source to ground will result in

$$V_{CC} - I_C R_C - V_{EB_1} - I_{B_1} R_B = 0$$

or

$$V_{CC} - V_{EB_1} - \beta_1 \beta_2 I_{B_1} R_C - I_{B_1} R_B = 0$$

and

$$I_{B_1} = \frac{V_{CC} - V_{EB_1}}{R_B + \beta_1 \beta_2 R_C} \quad (69)$$

The base voltage  $V_{B_1}$  is

$$V_{B_1} = I_{B_1} R_B \quad (70)$$

and

$$V_{B_2} = V_{BE_2} \quad (71)$$

The collector voltage  $V_{C_2} = V_{E_1}$  is

$$V_{C_2} = V_{CC} - I_C R_C \quad (72)$$

and

$$V_{C_1} = V_{BE_2} \quad (73)$$

In this case

$$V_{CE_2} = V_{C_2} \quad (74)$$

and

$$V_{EC_1} = V_{E_1} - V_{C_1}$$

so that

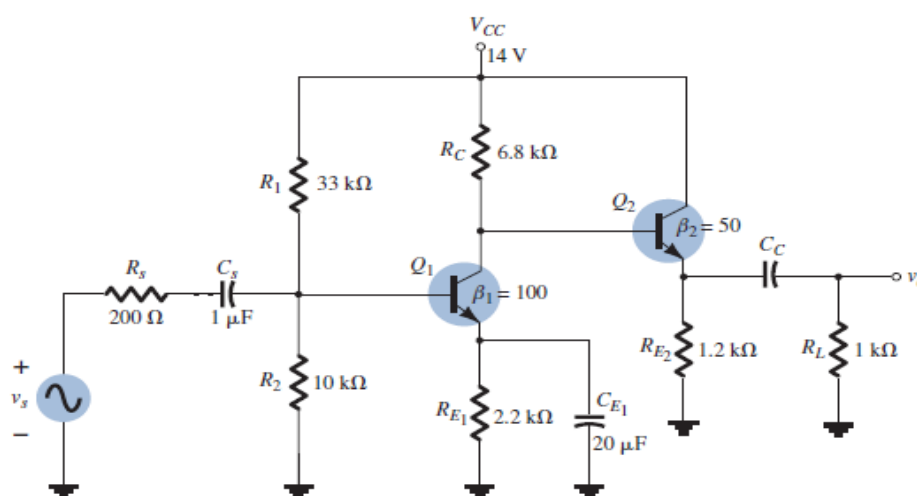
$$V_{EC_1} = V_{C_2} - V_{BE_2} \quad (75)$$

## 5. Direct Coupled Amplifier

The last multistage configuration to be introduced is the Direct Coupled amplifier such as appearing in Example 26. Note the absence of a coupling capacitor to isolate the dc levels of each stage. The dc levels in one stage will directly affect the dc levels in succeeding stages. The benefit is that the coupling capacitor typically limits the low-frequency response of the amplifier. Without coupling capacitors, the amplifier can amplify signals

of very low frequency—in fact down to dc. The disadvantage is that any variation in dc levels due to a variety of reasons in one stage can affect the dc levels in the succeeding stages of the amplifier.

**EXAMPLE 26** Determine the dc levels for the currents and voltages of the direct-coupled amplifier of Fig. 72. Note that it is a voltage-divider bias configuration followed by a common-collector configuration; one that is excellent in cases wherein the input impedance of the next stage is quite low. The common-collector amplifier is acting like a buffer between stages.



**FIG. 72**  
Direct-coupled amplifier.

**Solution:** The dc equivalent of Fig. 72 appears as Fig. 73. Note that the load and source are no longer part of the picture. For the voltage-divider configuration, the following equations for the base current were developed in Section 5.

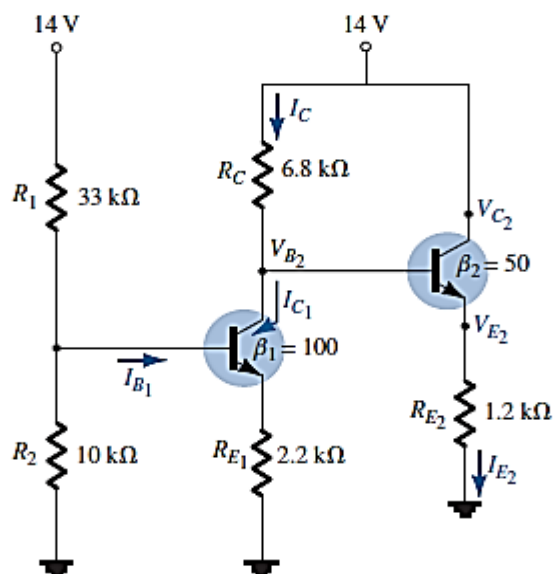
$$I_{B_1} = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_{E_1}}$$

with

$$R_{Th} = R_1 \parallel R_2$$

and

$$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$$



**FIG. 73**  
DC equivalent of Fig. 72.

In this case,

$$R_{Th} = 33\text{ k}\Omega \parallel 10\text{ k}\Omega = 7.67\text{ k}\Omega$$

and

$$E_{Th} = \frac{10\text{ k}\Omega(14\text{ V})}{10\text{ k}\Omega + 33\text{ k}\Omega} = 3.26\text{ V}$$

so that

$$\begin{aligned} I_{B1} &= \frac{3.26\text{ V} - 0.7\text{ V}}{7.67\text{ k}\Omega + (100 + 1)2.2\text{ k}\Omega} \\ &= \frac{2.56\text{ V}}{229.2\text{ k}\Omega} \\ &= 11.17\text{ }\mu\text{A} \end{aligned}$$

with

$$\begin{aligned} I_{C1} &= \beta I_{B1} \\ &= 100(11.17\text{ }\mu\text{A}) \\ &= 1.12\text{ mA} \end{aligned}$$

In Fig. 73 we find that

$$V_{B2} = V_{CC} - I_{C1}R_{C1} \quad (76)$$

$$\begin{aligned} &= 14\text{ V} - (1.12\text{ mA})(6.8\text{ k}\Omega) \\ &= 14\text{ V} - 7.62\text{ V} \\ &= 6.38\text{ V} \end{aligned}$$

and

$$\begin{aligned} V_{E2} &= V_{B2} - V_{BE2} \\ &= 6.38\text{ V} - 0.7\text{ V} \\ &= 5.68\text{ V} \end{aligned}$$

$$\begin{aligned}
 &= 14 \text{ V} - (1.12 \text{ mA})(6.8 \text{ k}\Omega) \\
 &= 14 \text{ V} - 7.62 \text{ V} \\
 &= 6.38 \text{ V}
 \end{aligned}$$

and

$$\begin{aligned}
 V_{E_2} &= V_{B_2} - V_{BE_2} \\
 &= 6.38 \text{ V} - 0.7 \text{ V} \\
 &= 5.68 \text{ V}
 \end{aligned}$$

resulting in

$$I_{E_2} = \frac{V_{E_2}}{R_{E_2}} \quad (77)$$

$$\begin{aligned}
 &= \frac{5.68 \text{ V}}{1.2 \text{ k}\Omega} \\
 &= 4.73 \text{ mA}
 \end{aligned}$$

Obviously,

$$V_{C_2} = V_{CC} \quad (78)$$

$$= 14 \text{ V}$$

and

$$V_{CE_2} = V_{C_2} - V_{E_2}$$

$$V_{CE_2} = V_{CC} - V_{E_2} \quad (79)$$

$$\begin{aligned}
 &= 14 \text{ V} - 5.68 \text{ V} \\
 &= 8.32 \text{ V}
 \end{aligned}$$

## 4.11 CURRENT MIRRORS

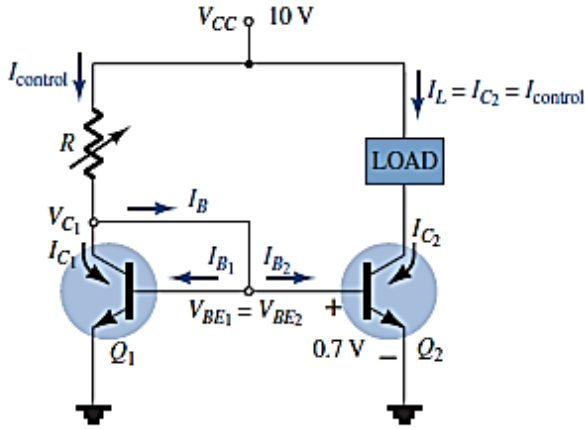
The **current mirror** is a dc network in which the current through a load is controlled by a current at another point in the network. That is, if the controlling current is raised or lowered the current through the load will change to the same level.

The discussion to follow will demonstrate that the effectiveness of the design is dependent on the fact that the two transistors employed have identical characteristics. The basic configuration appears in Fig. 74. Note that the two transistors are back-to-back and the collector of one is connected to the base of the two transistors. Assume identical transistors will result in  $V_{BE1} = V_{BE2}$  and  $I_{B1} = I_{B2}$  as defined by the base-to-emitter characteristics of Fig. 75. Raise the base to emitter voltage, and the current of each will rise to the same value.

Since the base to emitter voltages of the two transistors in Fig. 74 are in parallel, they must have the same voltage. The result is that  $I_{B1} = I_{B2}$  at every set base to emitter voltage. It is clear from Fig. 74 that  $I_B = I_{B1} + I_{B2}$

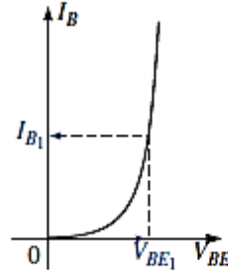
and if  $I_{B1} = I_{B2}$

then  $I_B = I_{B1} + I_{B2} = 2I_{B1}$



**FIG. 74**

Current mirror using back-to-back BJTs.



**FIG. 75**

Base characteristics for transistor  $Q_1$  (and  $Q_2$ ).

In addition,

$$I_{\text{control}} = I_{C1} + I_B = I_{C1} + 2I_{B1}$$

but

$$I_{C1} = \beta_1 I_{B1}$$

so

$$I_{\text{control}} = \beta_1 I_{B1} + 2I_{B1} = (\beta_1 + 2)I_{B1}$$

and since  $\beta_1$  is typically  $\gg 2$ ,  $I_{\text{control}} \cong \beta_1 I_{B1}$

or

$$I_{B1} = \frac{I_{\text{control}}}{\beta_1} \quad (80)$$

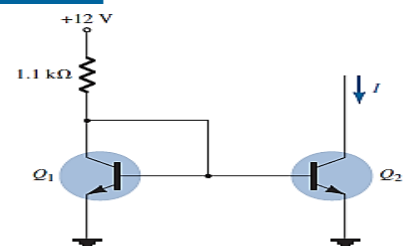
If the control current is raised, the resulting  $I_{B1}$  will increase as determined by Eq. 80. If  $I_{B1}$  increases, the voltage  $V_{BE1}$  must increase as dictated by the response curve of Fig. 75. If  $V_{BE1}$  increases, then  $V_{BE2}$  must increase by the same amount and  $I_{B2}$  will also increase. The result is that  $I_L = I_{C2} = \beta I_{B2}$  will also increase to the level established by the control current. Referring to Fig. 74 we find the control current is determined by

$$I_{\text{control}} = \frac{V_{CC} - V_{BE}}{R} \quad (81)$$

**EXAMPLE 27** Calculate the mirrored current  $I$  in the circuit of Fig. 76.

**Solution:** Eq. (75):

$$I = I_{\text{control}} = \frac{V_{CC} - V_{BE}}{R} = \frac{12 \text{ V} - 0.7 \text{ V}}{1.1 \text{ k}\Omega} = 10.27 \text{ mA}$$



**FIG. 76**

Current mirror circuit for Example 27.

**EXAMPLE 28** Calculate the current  $I$  through each of the transistor  $Q_2$  and  $Q_3$  in the circuit of Fig. 77.

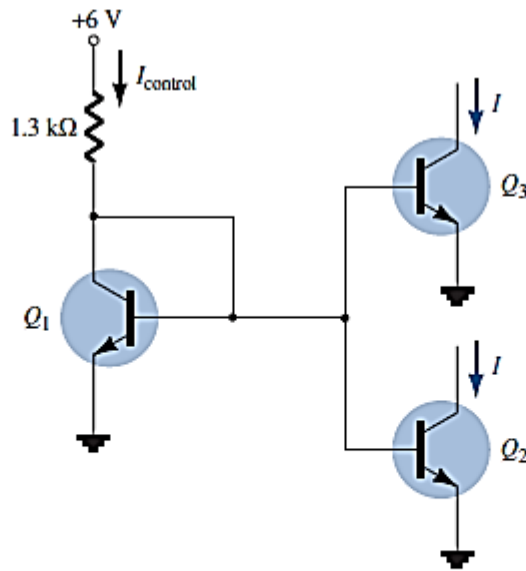
**Solution:** Since  $V_{BE_1} = V_{BE_2} = V_{BE_3}$  then  $I_{B_1} = I_{B_2} = I_{B_3}$

Substituting  $I_{B_1} = \frac{I_{\text{control}}}{\beta}$  and  $I_{B_2} = \frac{I}{\beta}$  with  $I_{B_3} = \frac{I}{\beta}$

we have  $\frac{I_{\text{control}}}{\beta} = \frac{I}{\beta} = \frac{I}{\beta}$

so  $I$  must equal  $I_{\text{control}}$

and  $I_{\text{control}} = \frac{V_{CC} - V_{BE}}{R} = \frac{6\text{ V} - 0.7\text{ V}}{1.3\text{ k}\Omega} = 4.08\text{ mA}$



**FIG. 77**

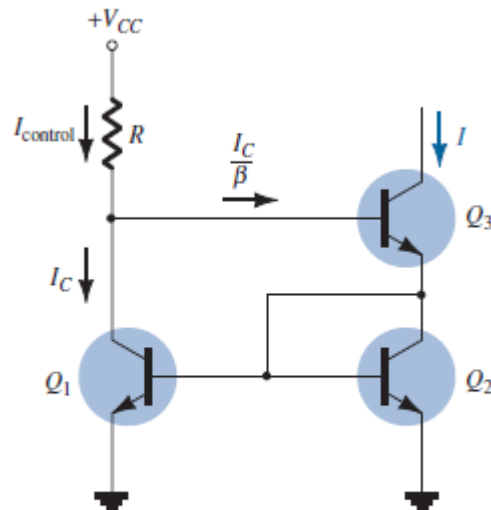
Current mirror circuit for Example 28.

Figure 78 shows another form of current mirror to provide higher output impedance than that of Fig. 74. The control current through  $R$  is

$$I_{\text{control}} = \frac{V_{CC} - 2V_{BE}}{R} \approx I_C + \frac{I_C}{\beta} = \frac{\beta + 1}{\beta} I_C \approx I_C$$

Assuming that  $Q_1$  and  $Q_2$  are well matched, we find that the output current  $I$  is held constant at  $I \approx I_C = I_{\text{control}}$

Again we see that the output current  $I$  is a mirrored value of the current set by the fixed current through  $R$ .

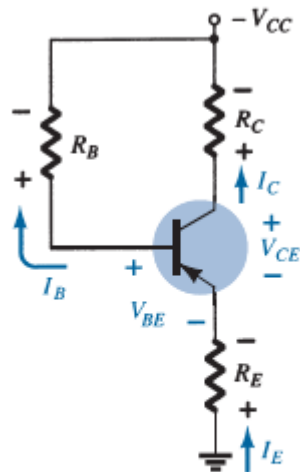
**FIG. 78**

*Current mirror circuit with higher output impedance.*

## 4.12 PNP TRANSISTORS

The analysis thus far has been limited totally to *npn* transistors to ensure that the initial analysis of the basic configurations was as clear as possible and uncomplicated by switching between types of transistors. Fortunately, the analysis of *pnp* transistors follows the same pattern established for *npn* transistors. The level of  $I_B$  is first determined, followed by the application of the appropriate transistor relationships to determine the list of unknown quantities.

In fact, the only difference between the resulting equations for a network in which an *npn* transistor has been replaced by a *pnp* transistor is the sign associated with particular quantities. As noted in Fig. 85, the double-subscript notation continues as normally defined. The current directions, however, have been reversed to reflect the actual conduction directions. Using the defined polarities of Fig. 85, both  $V_{BE}$  and  $V_{CE}$  will be negative quantities. Applying Kirchhoff's voltage law to the base–emitter loop results in the following equation for the network of Fig. 85:



**FIG. 85**  
*pnp transistor in an emitter-stabilized configuration.*

Substituting  $I_E = (\beta + 1)I_B$  and solving for  $I_B$  yields

$$I_B = \frac{V_{CC} + V_{BE}}{R_B + (\beta + 1)R_E} \quad (84)$$

The resulting equation is the same as Eq. (17) except for the sign for  $V_{BE}$ . However, in this case  $V_{BE} = -0.7$  V and the substitution of values results in the same sign for each term of Eq. (84) as Eq. (17). Keep in mind that the direction of  $I_B$  is now defined opposite of that for a *pnp* transistor as shown

in Fig. 85. For  $V_{CE}$  Kirchhoff's voltage law is applied to the collector–emitter loop, resulting in the following equation:

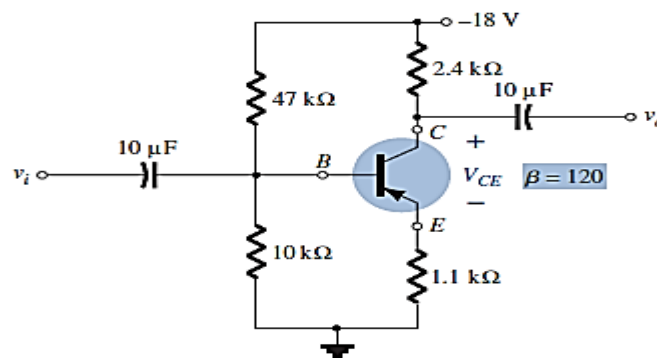
$$-I_E R_E + V_{CE} - I_C R_C + V_{CC} = 0$$

Substituting  $I_E \approx I_C$  gives

$$V_{CE} = -V_{CC} + I_C(R_C + R_E) \quad (85)$$

The resulting equation has the same format as Eq. (19), but the sign in front of each term on the right of the equal sign has changed. Because  $V_{CC}$  will be larger than the magnitude of the succeeding term, the voltage  $V_{CE}$  will have a negative sign, as noted in an earlier paragraph.

**EXAMPLE 31** Determine  $V_{CE}$  for the voltage-divider bias configuration of Fig. 86.



**FIG. 86**  
*pnp transistor in a voltage-divider bias configuration.*



**Solution:** Testing the condition

$$\beta R_E \geq 10R_2$$

results in

$$\begin{aligned}(120)(1.1 \text{ k}\Omega) &\geq 10(10 \text{ k}\Omega) \\ 132 \text{ k}\Omega &\geq 100 \text{ k}\Omega \quad (\text{satisfied})\end{aligned}$$

Solving for  $V_B$ , we have

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(10 \text{ k}\Omega)(-18 \text{ V})}{47 \text{ k}\Omega + 10 \text{ k}\Omega} = -3.16 \text{ V}$$

Note the similarity in format of the equation with the resulting negative voltage for  $V_B$ .

Applying Kirchhoff's voltage law around the base-emitter loop yields

$$+V_B - V_{BE} - V_E = 0$$

and

$$V_E = V_B - V_{BE}$$

Substituting values, we obtain

$$\begin{aligned}V_E &= -3.16 \text{ V} - (-0.7 \text{ V}) \\ &= -3.16 \text{ V} + 0.7 \text{ V} \\ &= -2.46 \text{ V}\end{aligned}$$

Note in the equation above that the standard single- and double-subscript notation is employed. For an *npn* transistor the equation  $V_E = V_B - V_{BE}$  would be exactly the same. The only difference surfaces when the values are substituted.

The current is

$$I_E = \frac{V_E}{R_E} = \frac{2.46 \text{ V}}{1.1 \text{ k}\Omega} = 2.24 \text{ mA}$$

For the collector-emitter loop,

$$-I_E R_E + V_{CE} - I_C R_C + V_{CC} = 0$$

Substituting  $I_E \cong I_C$  and gathering terms, we have

$$V_{CE} = -V_{CC} + I_C(R_C + R_E)$$

Substituting values gives

$$\begin{aligned}V_{CE} &= -18 \text{ V} + (2.24 \text{ mA})(2.4 \text{ k}\Omega + 1.1 \text{ k}\Omega) \\ &= -18 \text{ V} + 7.84 \text{ V} \\ &= -10.16 \text{ V}\end{aligned}$$